J2103A

Power Stage Isolator

Operation Manual

Version 1.0 Dated: 05/14/2023

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1. Introduction to J2103A

All electronic products, whether powered by mains or batteries, contain power regulation circuits that can use switching or linear power supplies, or both. Feedback control circuits are necessary to stabilize the output voltage of both types of power supplies. Therefore, the design of feedback control circuits has always been a focal point for young power engineers to learn. However, before designing the correct feedback control circuit, power engineers need to understand the frequency response of the power output circuit (Power stage) to be controlled.

In the past, we would use simulation tools with circuit models to analyze the power supply and predict the frequency response of the power stage. Then, we would proceed with the first feedback control circuit design. If the circuit worked properly, we could use a Frequency Response Analyzer (FRA) or Vector Network Analyzer (VNA) and an injection transformer to measure the frequency response of the power output circuit (Power stage) and optimize the feedback control circuit according to the measurement results. However, the whole process can be very time-consuming and cumbersome.

The J2103A Power Stage Isolator is a device that replaces feedback control circuits to control the power output circuit (Power stage), also, known as the power stage plant. The power supply plant gain represents the amplification factor of the power supply unit within this feedback control loop. With the J2103A, we can measure the frequency response of the power output circuit (Power stage) before designing the feedback control circuit and design the feedback control circuit according to the actual measurement results. The whole design process is almost done at one time, and the integration of the power output circuit (Power stage) and the feedback control circuit is relatively accurate and greatly shortens the design cycle.

The J2103A can be used in almost any power circuit that requires feedback control. Its feedback input (Vin) and reference voltage (Vref) use differential inputs without reference ground problems. Therefore, designs with isolated or non-isolated power sources, switching or linear power supplies, and positive or negative voltage feedback can all use J2103A.

2. J2103A Package Contents

Figure 1 displays the product contents. The J2103A includes...

a. J2103A unit x 1 (includes a battery)
b. Type C charging cable x 1
c. PWR-OPT03Banana to USB adapter x 1
d. Dupont testing cables x 2

Figure 1 J2103A Product Contents

Note 1: For battery transportation, please refer to the lithium battery product transportation regulations in "The shipping regulations for lithium batteries.pdf."

Note 2: For more information on the banana plug to USB adapter, please refer to the PWR-OPT03 user manual in "Banana to USB Connecter1.pdf."

3. Side Panel Configuration 1

The configuration diagram of panel 1 for J2103A is shown in Figure 2.

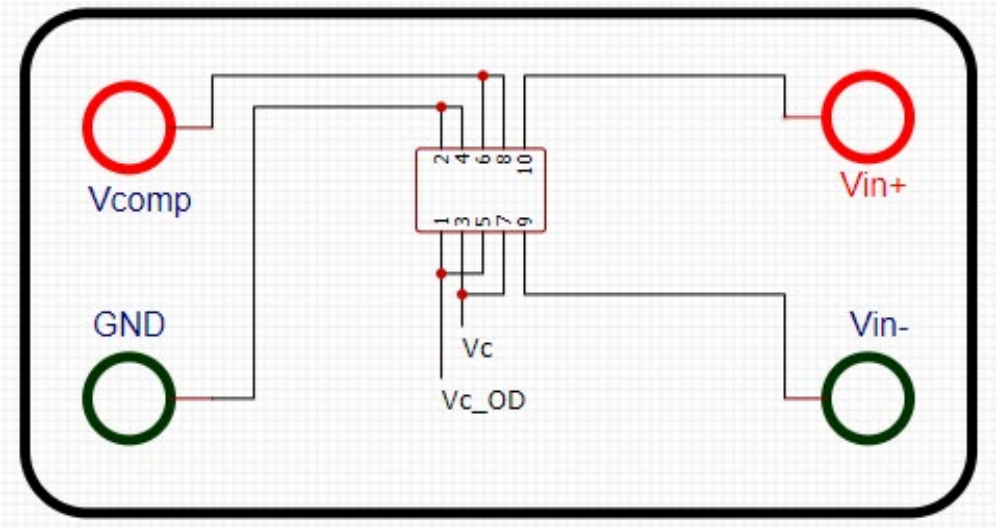

Figure 2 J2103A Panel Configuration I

According to Figure 2, the J2103A provides two types of input/output ports: Banana jacks and Dupont connectors:

a. You can select the Vcomp output using the Dupont terminals. By connecting pin 5 to pin 6 with a jumper capacitor, you can set Vcomp to open drain output. Alternatively, by connecting pin 7 to pin 8, you can set Vcomp to a push-pull output. The factory setting for Vcomp is for a push-pull output.
b. Vin (Vin+, Vin-), and Vref(Vref+, Vref-) are the differential inputs, and Vin- and Vref- are not referenced to the GND port.
c. The Vcomp open drain output can be connected to the Dupont cable output by using the Dupont terminal pin 1 (Vc_OD) and pin 2 (GND).
d. The Vcomp push-pull output can be connected to the Dupont cable output by using the Dupont terminal pin 3 (Vc) and pin 4 (GND).
e. Vin can be connected to the Dupont line input by using the Dupont terminal pin 10 (Vin+) and pin

4. Side Panel Configuration 2

The configuration diagram of panel 2 for the J2103A is shown in Figure 3.

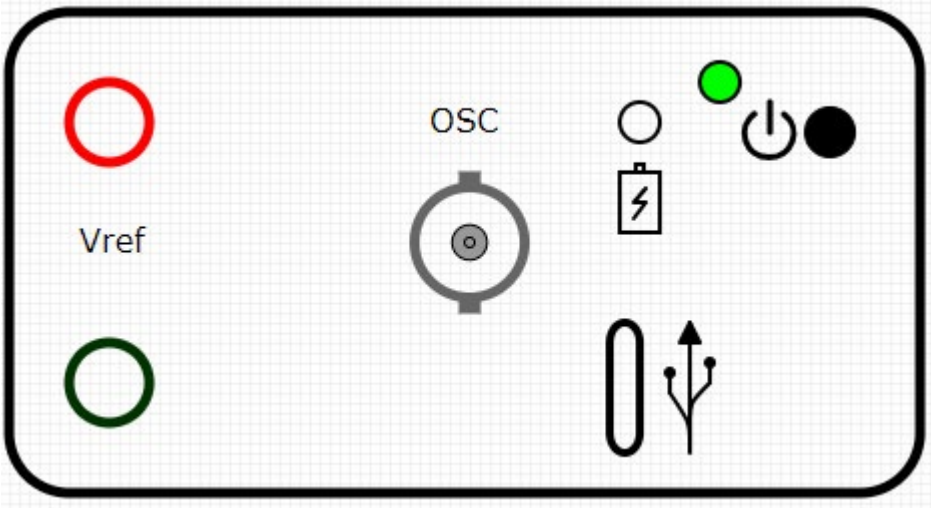

Figure 3 J2103A Panel Configuration 2

Figure 3-1 Power Indicator Lights

Figure 3-1 shows the Power indicator lights:

a. **Green light constantly on:** Power ON indicator light.
b. **Green light off:** Power OFF state.
c. **Flashing orange light:** Indicates low battery voltage (automatic power-off after 5-10 minutes).

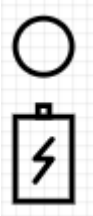

Figure 3-2 Battery Charging Lights

Figure 3-2 shows the Battery charging indicator lights:

a. **Red light constantly on:** Constant current charging.
b. **Orange and Red LED alternating flashing:** Constant voltage charging.
c. **Green light constantly on:** Charging complete.
d. **Flashing red light:** Trickle charging (0.5 seconds on/0.5 seconds off).

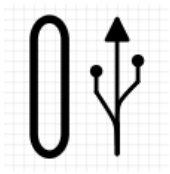

Figure 3-3 USB Type-C Charging Port

The USB Type-C charging port shown on Figure 3-3 is for charging only. When J2103A is being charged, the power switch will automatically turn off and cannot be operated. A 5V, 15W USB charger adapter can be used as the charging power source, **or the included USB to banana adaptor (PWR-OPT03) can be used along with a general desktop DC power supply set to output 5V and limit the current to 3A**

5. J2103A Operation Steps

Figure 4 shows the circuit diagram of J2103A as connected to a DUT and FRA. Please operate according to the following instructions.

a. Turn off the DC power supplies A, B, and the J2103A power.
b. Configure the DUT to be controlled by the J2103A.
c. Connect the input terminal (Vin) of the J2103A to the output terminal of the DUT.
d. Connect the output terminal (Vcomp) of the J2103A to the control terminal of the DUT.
e. Connect the reference terminal (Vref) of the J2103A to DC power supply B.
f. Turn on the J2103A and DC power supply B and set Vref to 0V.
g. Turn on DC power supply A and set the input voltage of the DUT.
h. Adjust the Vref voltage until the output voltage of the DUT is equal to the target voltage, Vout=Vref x 10.
i. Measure the power stage gain using FRA or VNA. The disturbance signal can be injected through

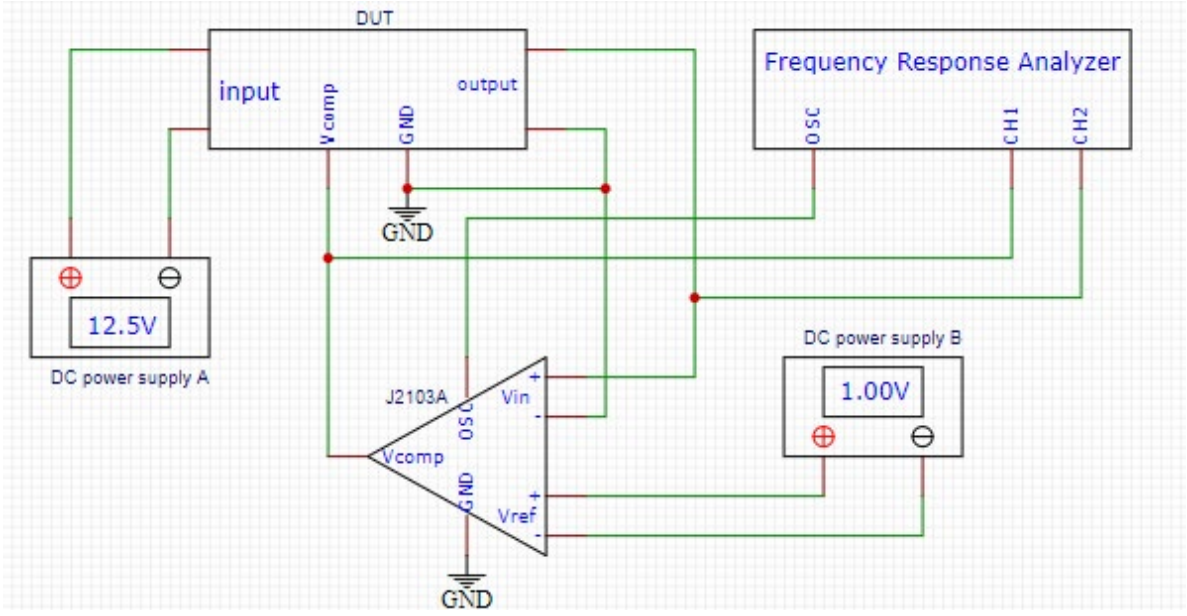

Figure 4 The General Circuit Diagram Using the J2103A to measure gain.

6. The OSC Signal Level for the J2103A

a. The OSC port has an input impedance of 50ohm.
b. The maximum input signal allowed is +26dBm, and the voltage of 4.46Vrms (12.6Vpk-pk).
c. There is an OSC to Vcomp port signal attenuation ratio of 20dB.

The J2103A operates with a single power supply, and the Vcomp output range is 0~10V. Therefore, the strength of the OSC signal, represented by Vosc/10, must be lower than the DC bias value of Vcomp under no clamp condition. Figure 5 and Figure 6 show the waveforms with Vcomp_DC = 200mV and Vosc = 10dBm (2Vpk-pk) and Vcomp_DC=50mV, Vosc=10dBm(2Vpk-pk).

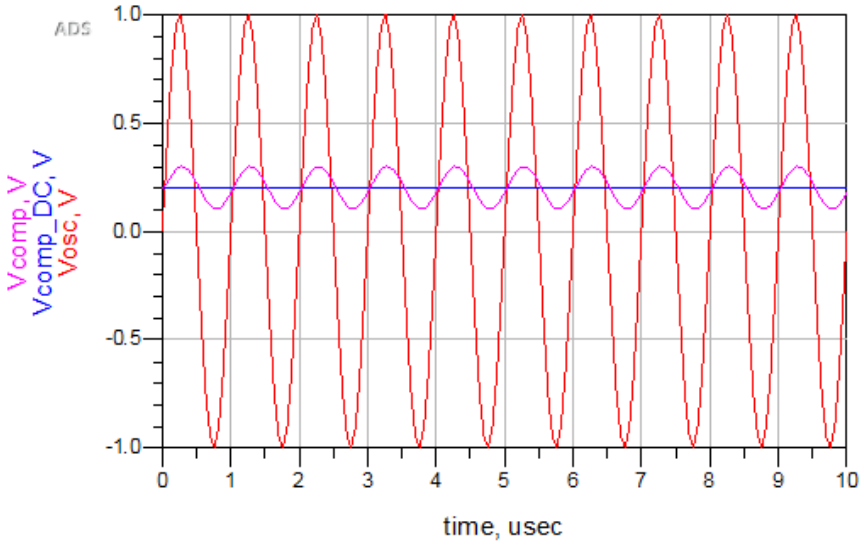

Figure 5 Vcomp_DC=200mV, Vosc=10dBm(2Vpk-pk)

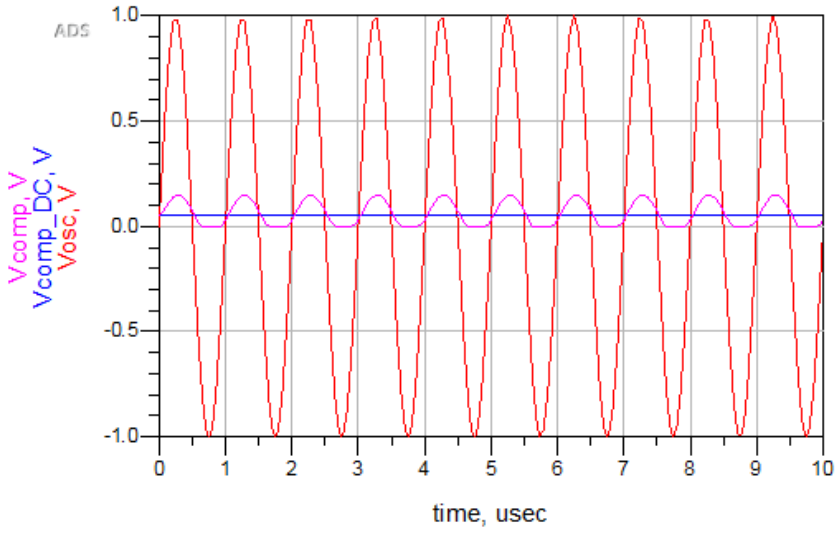

Figure 6. Vcomp_DC=50mV, Vosc=10dBm(2Vpk-pk)

7. Specifications

Here are some specifications related to the J2103A:

a. The Vref port is a differential input with a common mode input impedance of 10 kohm. The maximum input voltage is +/- 10V.
b. The Vin port is a differential input with a common mode input impedance of 100 kohm. The maximum input voltage is +/- 60V.
c. The OSC port is a single-ended input with an input impedance of 50 ohm. The maximum input power is +26dBm, and there is a 20dB attenuation from OSC to Vcomp. The bandwidth is greater than 1MHz.
d. Four LTO batteries are connected in series to power the J2103A. They can be fully charged in about 30 minutes and can work continuously for more than 8 hours with Vcomp=10V at no-load and the OSC port not connected.
e. At a frequency of 10Hz, the gain is approximately -48dB and the phase shift is 90 degrees.

8. Inspection

Figures 7 and 8 show the results of verifying the frequency response of Vin to Vcomp and OSC to Vcomp using an E5061B network analyzer.

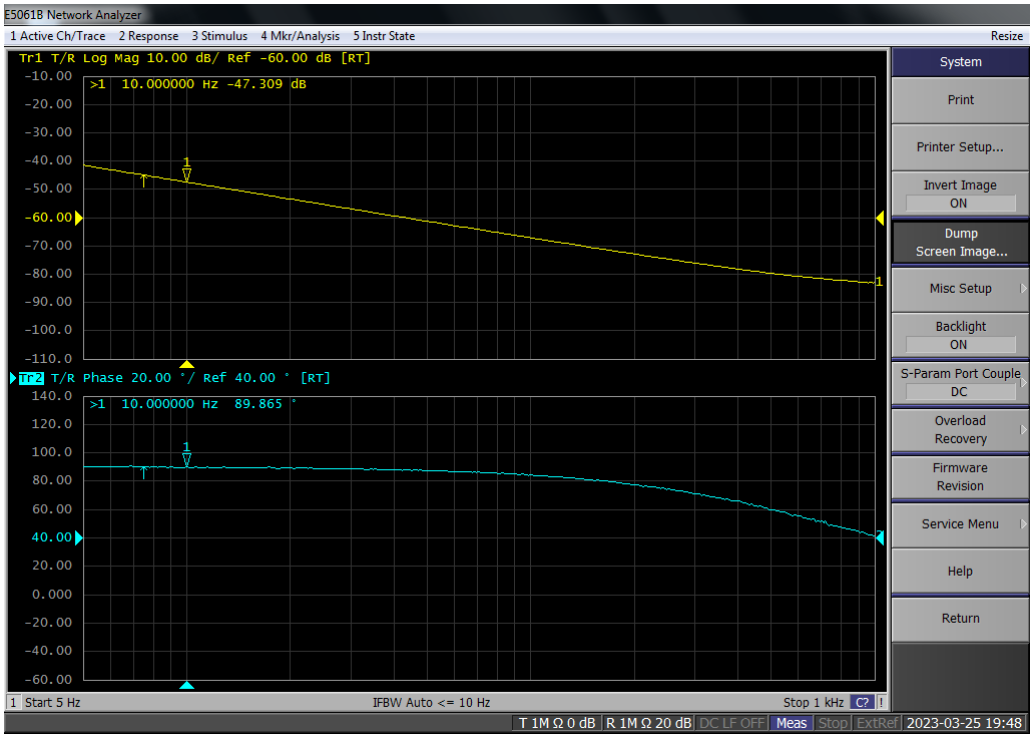

Figure 7 Frequency response of Vin to Vcomp

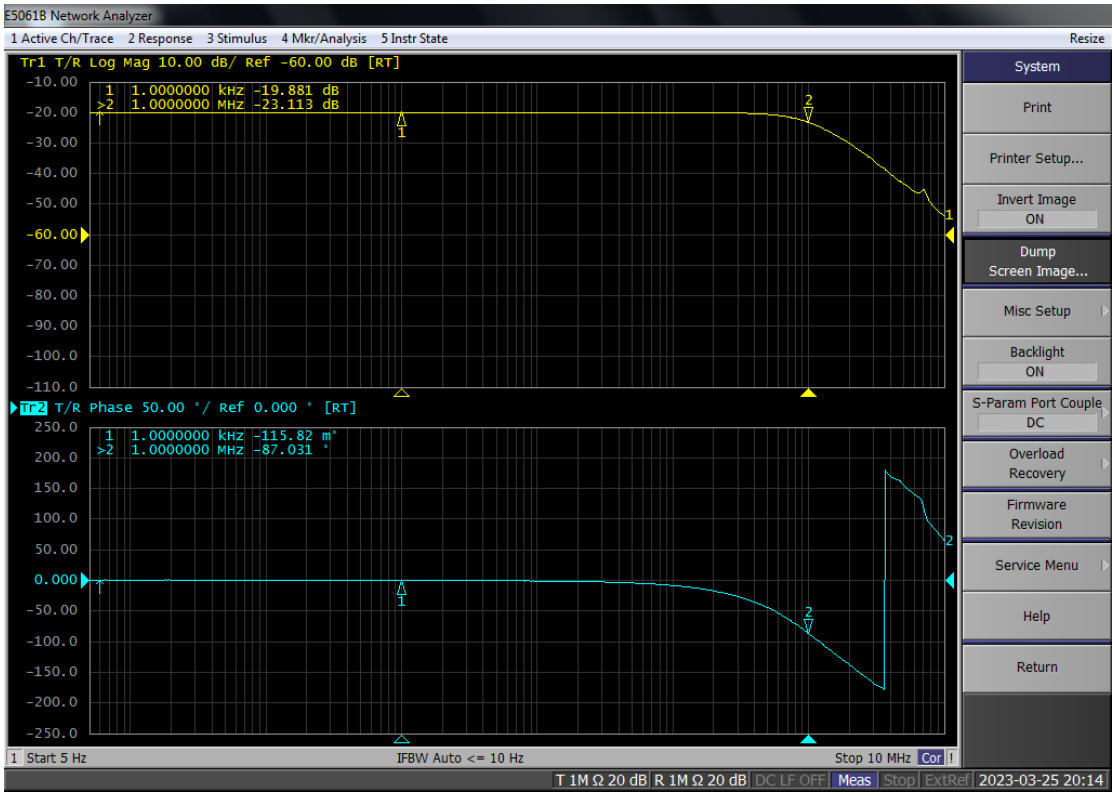

Figure 8 Frequency response of OSC to Vcomp